A TUDOMÁNYOS KUTATÁSOK KIBONTAKOZTATÁSA
A PÁZMÁNY PÉTER KATOLIKUS EGYETEMEN
TÁMOP-4.2.1.B-11/2/KMR-2011-0002

NEW SZÉCHENYI PLAN

Pázmány Péter Catholic University

Array and multi-processor architectures

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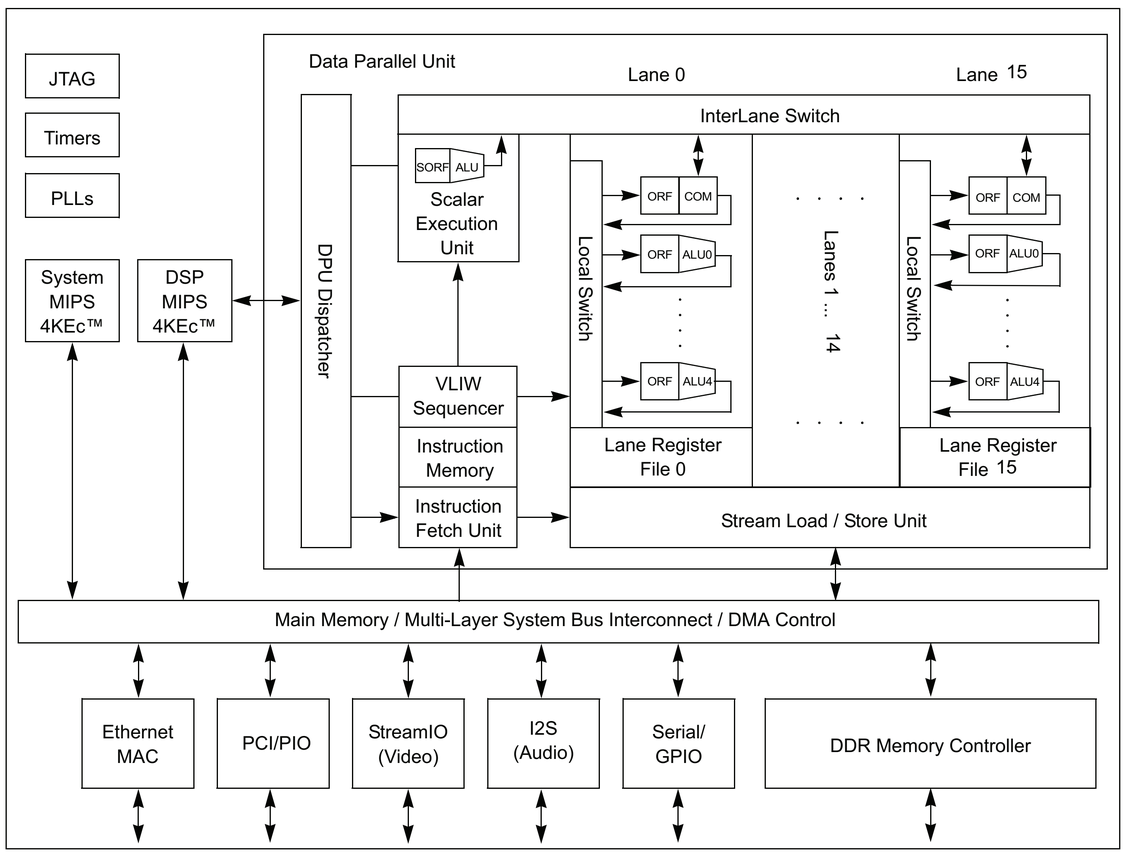
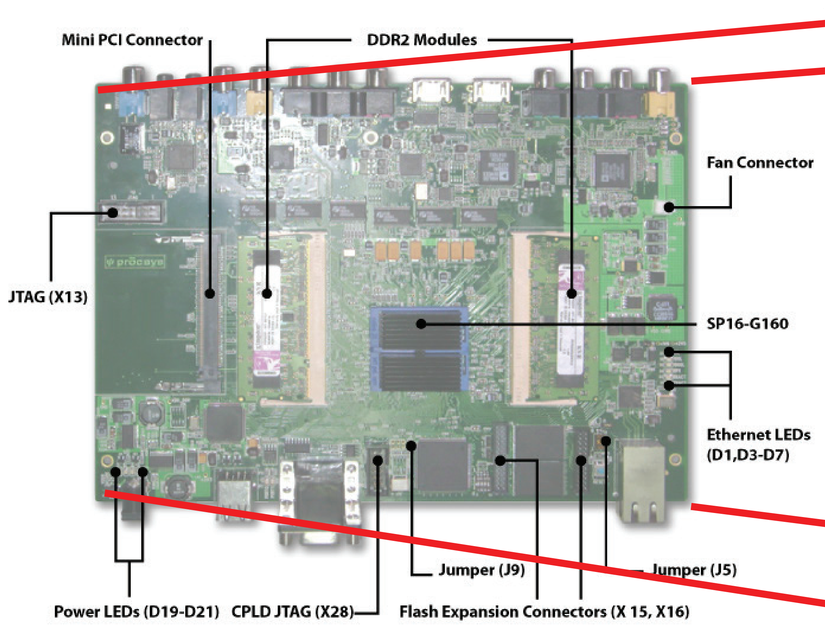
Stream Processor Archicecture

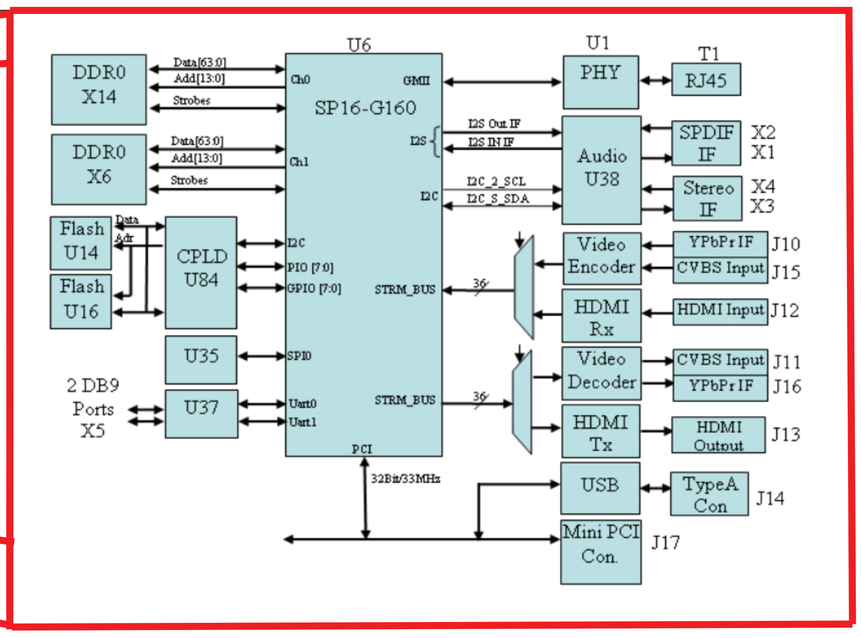


SP16-G160

- High-performance DSP subsystem
  - 16 data-parallel processing lanes with five VLIW ALUs each; 160 GOPS and 80 GMACS (16 x 16 -bit data) at 500 MHz
  - 32-bit MIPS 4KEc core, 250 MHz
- System CPU
  - 32-bit MIPS 4KEc core, 250 MHz
- Internal 24 GBytes/s interconnect bus
- Stream processor architecture
  - Compiler automation of DMA and allocation of on-chip memory with runtime synchronization of memory transfer and kernel execution in hardware
  - Single-flow VLIW execution across data-parallel processing lanes
  - Distributed register hierarchy that optimizes data locality and minimizes off-chip memory transfers
  - Massively parallel execution across SIMD lanes
  - Flexible data load/store DMA hardware that supports complex memory access patterns
  - Coarse-grained parallelism with concurrent data load and kernel function execution
- On-Chip memory
  - 256 KBytes Lane Register Files
  - 19 KBytes Operand Register Files
  - 96 KBytes VLIW instruction memory
  - 2x16/16 KBytes data/instr MIPS caches

Stream Processing Evaluation Platform





- Example applications
  - Video security: Intelligent video servers, DVRs
  - Video conferencing: HD H.264 systems
  - Broadcasting: Headends
  - Image processing: Printers/MFPs
  - Medical imaging

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HUNGARY'S RENEWAL

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